Exhibit 39

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

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EMC CORPORATION,

Petitioner,

v.

ACQIS LLC,

Patent Owner.

_____

Case IPR2014-01462 (Patent 8,041,873 B2)

Case IPR2014-01469 (Patent RE42,814 E)

Thursday, August 27, 2015

Volume I of II

Deposition of VOLKER LINDENSTRUTH, taken at the offices of Gibson, Dunn & Crutcher, Carmelite House, 50 Victoria Embankment, London EC4Y 0DZ, beginning at 8:57 a.m. before Audrey Shirley, QRR, ACR, MBIVR.

Q. So that's the way you read this northbridge limitation, the way you've just explained it then? 12:05:07 12:05:08 12:05:11

A. (The witness nodded.) 12:05:13

Q. Okay. Now, the claim says that you have to communicate address and data bits. You would agree with me that it doesn't mention command information, correct? 12:05:14 12:05:17 12:05:22 12:05:25

MR. DAVIS: Objection to form. 12:05:28

THE WITNESS: It says: 12:05:31

"... address and data bits of PCI transaction in serial form ..." 12:05:34 12:05:37

It doesn't say explicitly the other corollary information which is needed to define a PCI transaction, but it says "PCI transaction". So without, for instance, the additional functionality, it wouldn't be a PCI transaction. 12:05:38 12:05:41 12:05:44 12:05:48 12:05:55

BY MR. BUROKER: 12:06:10

Q. So even though the word "command information" is not expressly present, it's your reading of this claim that the northbridge must communicate PCI bus command information in serial form as well; is that correct? 12:06:10 12:06:12 12:06:15 12:06:20 12:06:24

A. If you read this patent you will find that this context is defined as such. It is 12:06:28 12:06:30

question. 01:26:55

A. That's fine, don't worry. I did 01:26:56

not think I should. 01:26:58

Q. I have a question going back to 01:26:59

the PCI specification document. You were looking 01:27:02

I believe at page 36 at the read transaction as 01:27:04

an example of a transaction. 01:27:06

MR. DAVIS: Are you pointing at page 36 01:27:21

of the document? 01:27:23

MR. BUROKER: Oh, I'm sorry 36 of the 01:27:25

document, which is page 52 of the exhibit. It's 01:27:27

the 3.3.1 Read Transaction section. 01:27:30

A. Okay, this the one. 01:27:56

Q. Okay, so we were looking at this 01:27:58

earlier this morning, correct? 01:28:01

A. Yes. 01:28:02

Q. Are some of the elements along the 01:28:10

left-hand side called control lines in the PCI 01:28:11

specification? 01:28:14

A. I would consider them as such, 01:28:21

whether they are explicitly called control 01:28:23

signals I would have to check. But basically in 01:28:26

bus terminology you have the address, the data 01:28:33

and then additional corollary signals which 01:28:38

basically define what's going on, right? And 01:28:42

those constitute, in this case, the combined byte enables, then the initiator ready, target ready -- IRDY and TRDY -- which are basically used for the flow control, and the device select which is used for enabling the device to claim its existence in the bus. 01:28:44 01:28:49 01:28:53 01:28:58 01:29:01 01:29:04

Q. What is the "frame#" what is that? 01:29:05

A. And frame, of course, excuse me. 01:29:09

The frame. The frame signal is there to define the length of the transaction. This is a very fundamental thing because, unlike in other cases, in particular typically in networks, where the length of the packet is basically submitted as one of the very first words in the head of the packet saying, "This is it" and, "This is how long it will be." In PCI this doesn't exist. So a target being connected has no way of knowing how long this transaction will end up being, right? It will only know here is an address and here is a command, what is going to happen? And the length of the transaction is determined by the length the frame signal is asserted and if you refer, for instance, to column 8, clock cycle 8, you see that there is one last data transfer when frame is already high. This is basically 01:29:10 01:29:14 01:29:17 01:29:21 01:29:24 01:29:27 01:29:29 01:29:31 01:29:35 01:29:37 01:29:41 01:29:44 01:29:46 01:29:48 01:29:52 01:29:56 01:30:00

here it's called the control signals, frame, target ready, initiator ready. There is in addition the stop signal which is not disclosed in this diagram, which enables a device to say, "Terminate the transaction, no point going further, illegal address", something like that. So there are other transactions showing that in this spec and then device select and ID select. 01:31:41 01:31:47 01:31:53 01:31:55 01:31:59 01:32:01 01:32:04 01:32:08

Q. Yeah, I said 37 but I think it says at the top of page 7, 47 pins not 37, right? 01:32:14 01:32:16

"The PCI interface requires a minimum of 47 pins for a target-only device and 49 pins for a master to handle data in addressing, interface control, arbitration and system functions." 01:32:18 01:32:20 01:32:24 01:32:28 01:32:30

Correct? 01:32:31

A. 37 seemed a bit low to me, yeah. 01:32:31

Q. Do these control lines, such as frame, target ready, and so forth, are they part of the PCI bus transaction as you understand that term in the claims of the patent? 01:32:35 01:32:42 01:32:47 01:32:50

MR. DAVIS: Objection; form. 01:32:58

BY MR. BUROKER: 01:32:59

Q. So, you know, earlier we were talking about what your understanding of the term 01:32:59 01:33:00

"PCI bus transaction", looking at paragraph 114, for example, of your declaration, and you stated claims require address and data phases of a PCI bus transaction, et cetera. Are these control lines also part of what the claims require as a PCI bus transaction? 01:33:03 01:33:06 01:33:10 01:33:17 01:33:19 01:33:26

A. Since they are required to define what is going on on the bus at any point in time, the answer is yes. They define the PCI transaction. If you, for example, would remove from one byte enable you have no way of knowing whether we are reading, writing, or what other functionality is to be executed. If you remove any of the flow control signals, you cannot steer the fact if a device is not immediately ready, which happens a lot. So they would have to be -- they define the transaction, so have to be there. 01:33:27 01:33:30 01:33:34 01:33:37 01:33:41 01:33:46 01:33:49 01:33:51 01:33:57 01:33:59 01:34:05

Q. Okay. Looking at claim 24 as an example again. 01:34:09 01:34:14

A. Just wait, wait, wait. And we are talking now '873? 01:34:20 01:34:21

Q. No, '814 Patent, claim 24. 01:34:36

The complete phrase that we were looking at talks about communicating address and data bits of PCI bus transaction in serial form. Do 01:34:36 01:34:38 01:34:47

signals which are obviously less than what we have here. The corollary to that technically would mean it would have to be at a higher rate in order to keep up. 01:40:28 01:40:32 01:40:37 01:40:40

Q. And while that information is being transmitted over the serial line, is it still a PCI bus transaction? 01:40:42 01:40:44 01:40:48

MR. DAVIS: Objection to form. 01:40:54

THE WITNESS: Here I would stick to the specification and one of the functionalities and features of a specification requires that compliant devices can communicate with each other directly. So with a serialized version of this, although the entire information may be there but in a different form, one could not connect directly a PCI compliant device for it to work, it would have to be reconverted into the ordinary or defined PCI format for this to work. 01:40:59 01:41:03 01:41:07 01:41:09 01:41:13 01:41:19 01:41:21 01:41:24 01:41:28 01:41:31

BY MR. BUROKER: 01:41:35

Q. So the claims, in your reading, contemplate some sort of transformation of the PCI bus transaction into a format that is serially transmitted and then, on the other end, it would be converted back into PCI bus transaction format? 01:41:35 01:41:38 01:41:43 01:41:48 01:41:53 01:41:58

MR. DAVIS: Objection; form. 01:41:58

THE WITNESS: The patent text outlines this in great detail, and this is the context in which I would read this claim. Because it has to be seen in the context of the patent. So yes. 01:42:01 01:42:04 01:42:06 01:42:12

BY MR. BUROKER: 01:42:17

Q. If you add information to the PCI bus transaction is that resulting set of data still a PCI bus transaction? 01:42:44 01:42:46 01:42:54

MR. DAVIS: Objection; form. 01:42:58

THE WITNESS: Can you be more specific? 01:43:01

BY MR. BUROKER: 01:43:03

Q. Right, so if there's 47 lines in a PCI bus transaction, if you add five additional lines of information for whatever reason, is the resulting 55-bit piece of information still a PCI bus transaction? 01:43:03 01:43:06 01:43:12 01:43:15 01:43:21

MR. DAVIS: Objection; form. 01:43:23

THE WITNESS: The game about standards is quite clear: what is in the standard is what it is, no more no less. So answering your question, I say what you have now is some superset of a PCI transaction, which would be part of something else. That additional information has no meaning with respect to the 01:43:28 01:43:29 01:43:33 01:43:37 01:43:42 01:43:44 01:43:47

that unlike the invention TNet requires new hardware? 02:59:25 02:59:30

MR. DAVIS: Objection; form. 02:59:32

THE WITNESS: Now, let me just check, are we discussing here in context of TNet or in context of SCI? I think this is TNet, right? 02:59:38 02:59:46 02:59:50

BY MR. BUROKER: 02:59:56

Q. Correct. 02:59:56

A. Right, so these interfaces here have to have quite a bit of functionality, there is no direct obvious one-to-one A-B-C-D kind of path as to how they are to be built. They have to be able to execute all the specified PCI transactions on the remote PCI bus, but these transactions do not exist inside the TNet system area network. There is on top of that an address translation which needs to be done in the peer system, let alone it being initialized and everything. For it to be performing there is typically a very large complexity of additional functionality needed for this to make any sense. So this is a highly complex ASIC. 02:59:57 03:00:02 03:00:06 03:00:13 03:00:16 03:00:21 03:00:24 03:00:28 03:00:31 03:00:35 03:00:39 03:00:43 03:00:47 03:00:51

What is outlined in this patent is complex also, but we are basically serializing the particular ongoing PCI transaction which is 03:00:57 03:00:59 03:01:03

being then made parallel on the far end again. This is a different thing, there is no address translation for instance involved and all the other things. We can go into details here, if you want, to make this more clear. 03:01:05 03:01:09 03:01:11 03:01:12 03:01:15

Q. But my -- strike that. 03:01:23

My question was more, on paragraph 97, for example, it talks about avoiding the requirement imposed by TNet of designing new bus interface devices and new device drivers, but do you agree that to implement the '814 patent you still have to create a new hardware system to serialize the PCI bus transaction on one end and then interpret it on the other to output the PCI bus transaction on the receiving end, right? 03:01:25 03:01:27 03:01:34 03:01:40 03:01:43 03:01:50 03:01:53 03:01:56 03:02:01

MR. DAVIS: Objection; form. 03:02:03

THE WITNESS: The '814 Patent outlines how to build the serializer, this is correct. 03:02:06 03:02:14

BY MR. BUROKER: 03:02:14

Q. So there is some new piece of hardware, software, whatever it is, the serializer is something new? 03:02:17 03:02:18 03:02:20

A. Not software, hardware. 03:02:21

Q. So in the '814 Patent the patent talks about the host interface controller and 03:02:51 03:02:57